On-chip interconnect evaluation on delay time increase by crosstalk

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On-Chip Interconnect Evaluation on Delay Time Increase by Crosstalk

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Abstract

This paper describes on-chip interconnect evaluation on the delay time increase by crosstalk. The new test configurations were applied to evaluate the impact of low-k materials and improved circuit techniques on the delay time increase by crosstalk. It is found that the reduction of Cl for low-k materials, organic and air gap, is effective in reducing the delay time increase by crosstalk. Also, it is experimentally verified that improved circuit techniques such as repeaters and variable pitch routers significantly reduce not only interconnect delay but also delay time increase by crosstalk.

Introduction

As the device dimension is scaled down, the circuit performance strongly depends on the non-scalability of interconnects. In the deep submicron regime, multilevel interconnects are designed with a high aspect ratio structure to reduce the wiring resistance. This approach results in the increase of the ratio of the lateral and vertical capacitance components Cl / Cv. It has been pointed out crosstalk is a serious problem on both signal noise [1]- [2] and delay time increase by crosstalk [3], using interconnect models.

The purpose of this paper is to present the methodology of on-chip interconnect evaluation on the delay time increase by crosstalk. In a previous work [4], a test structure for crosstalk was developed for noise analysis. Unfortunately, this approach has little impact on on-chip evaluation on delay time increase by crosstalk. New simple test configurations are developed to characterize the delay time increase by crosstalk. It is found that the reduction of Cl for low-k materials and the improved circuit design techniques such as repeaters and variable pitch routers are effective in reducing the delay time increase by crosstalk.

On-Chip Interconnect Evaluation

New test configurations consist of a ring oscillator with wire load as shown in Fig.1 (a). Three test patterns are developed for three signal phases (1) normal, (2) in-phase and (3) anti-phase as shown in Fig.1 (b). For in-phase, the gate is divided into fun out of 3 to drive 3 interconnects. For anti-phase, the additional inverter is required to generate the reverse signal phase on the outer lines. It is confirmed by circuit simulations that this inverter delay is negligible to investigate delay time increase by crosstalk on the center line. For a comparison between normal type and crosstalk type, inverter delay of fun out of 3 is taken into consideration. Fig.1 (c) shows the schematic layout and cross section of test configurations. Wire load is laid out by the second metal layer with two ground planes. Two neighbors of wire load are ground lines for normal type, and signal lines for crosstalk type. The parameters of line width L, space S and interconnect length Lint are summarized in Fig.1 (d). The minimum L and S are both 0.25μm. The variable pitches are 2 times and 3 times pitch, respectively. Interconnect length Lint is 0.5, 1, 2, 4 and 8mm to analyze the effect of the repeater. The number of the ring oscillator stage is varied from 9 to 51 stage corresponding to the interconnect length. The driver size of the inverter is set to be 15μm for NMOS and 30μm PMOS, respectively, assuming global interconnect.

Fig.2 shows a test chip die photograph. The test chip is 3.0 × 7.2 mm^2 die area and it consists of 45 measurable test structures. These test configurations were made of 0.18μm CMOS process and evaluated using a 2 level Al process. Gate length of the driver is 0.16μm. All measurements were carried out at the power supply voltage 2V. Measured ring oscillator waveforms of test configurations are shown for both normal and anti-phases in Fig.3 and for the materials of air gap [5] and SiO2 in Fig.4. The new test configurations exhibit the delay time increase by crosstalk and the impact of low-k material on delay time.

Fig.5 shows measured delay time versus interconnect length at different metal pitches. The delay time is drastically increased with the increase of the interconnect length. In particular, the delay time of 8mm interconnect length is more than 2ns for the narrowest pitch (L=S=0.25μm). The use of wider pitch significantly reduces the delay time. Crosstalk induces the delay time shift when outer lines are switching simultaneously. As shown in Fig.6, the delay time is increased for the anti-phase and decreased for the in-phase. This is because the effective capacitance Ceff is roughly estimated to be 2Cl + Cv for the normal case, Cv for in-phase and 4Cl + Cv for anti-phase, respectively. Here Cl and Cv are lateral and vertical capacitance components, respectively as shown in Fig. 7. A simple Sakurai's delay model [6] is available to check the validity of the test configurations. Here interconnect and transistor parameters are extracted by

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measured data. The simulated results are in good agreement with the measured data as shown in Figs. 5-6. The crosstalk effect is evaluated simply using these on-chip test configurations.

Result and Discussion

A. Low-k materials

The test configurations were applied to evaluate the reduction of the lateral wiring capacitance Cl using low-k materials using a 2 level Al with 0.18μm CMOS process (Fig.7). ILD processes with the materials of SiO2, organic, air-gap [5] and without ILD are compared. Dielectric constant of SiO2 and organic is 4.2 and 2.8, respectively. Effective dielectric constant of air-gap [6] is estimated to be less than 2.0. ILD material between 1st Al and 2nd Al is SiO2. Interlayer ILD thickness and Al thickness (including barrier metal) are 1.0μm and 0.5μm, respectively. These interconnect parameters used for experiments are summarized in Table.1.

Fig.8 shows measured wiring capacitance components, (a) lateral capacitance Cl and (b) vertical capacitance Cv for various ILD processes. Cl is decreased using low-k material. On the other hand, Cv is almost identical for various ILD processes due to the same ILD material between 1st Al and 2nd Al. Therefore the ratio between Cl and Cv, which enhances the crosstalk effect, is decreased using low-k material as shown in Fig.8 (c). The delay time is plotted as a function of 2Cl + Cv for (a) normal case and 4Cl + Cv for (b) anti-phase case, respectively (Fig.9). These delay times are proportional to the effective capacitance in corresponding to low-k material. The delay time increase by crosstalk, which is defined as the normalizing of the worst case delay time (anti-phase) by the normal delay time, is significantly decreased using low-k materials because of the reduction of Cl (Fig.10). It is verified the ratio between Cl and Cv exhibits a key parameter for the delay time increase by crosstalk.

B. Improved circuit techniques

It has been pointed out improved circuit techniques are very effective in reducing the interconnect delay and crosstalk effect [2]-[3]. For the first time, the effect of improved circuit techniques is experimentally demonstrated using the new test configurations. These test configurations reveal that improved circuit techniques such as repeaters and variable pitch routers are effective in reducing not only interconnect delay but also delay time increase by crosstalk as shown in Figs. 11-12. The repeater reduces effective interconnect length and the variable pitch router reduces the ratio between Cl and Cv. Here interconnect length is 8mm in case of without repeaters. For an example, the delay time of 8 repeaters corresponds to that of 1mm interconnect length multiplied by 8 times.

As shown in Fig.11, the repeaters significantly improve the delay time. The number of the repeater is enough to be 2 for the wider pitch and 4 for the narrower pitch. The delay time increase by crosstalk is monotonically reduced with the increase of the repeaters as shown in Fig. 12.

Conclusion

In conclusion, we have developed on-chip interconnect evaluation on the delay time increase by crosstalk. The new test configurations allow the evaluation of the delay time increase by crosstalk. It is demonstrated that the reduction of Cl for low-k materials, organic and air-gap, is effective in reducing the delay time increase by crosstalk. It is clarified that improved circuit techniques such as repeaters and variable pitch routers significantly reduce not only interconnect delay but also delay time increase by crosstalk. The on-chip interconnect estimation allows us to evaluate the crosstalk effect on complex structures of low-k materials and improve circuit techniques.

Acknowledgment

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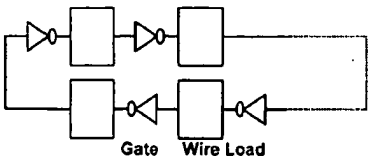
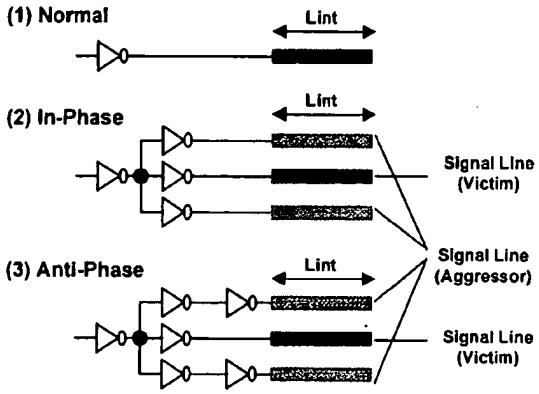
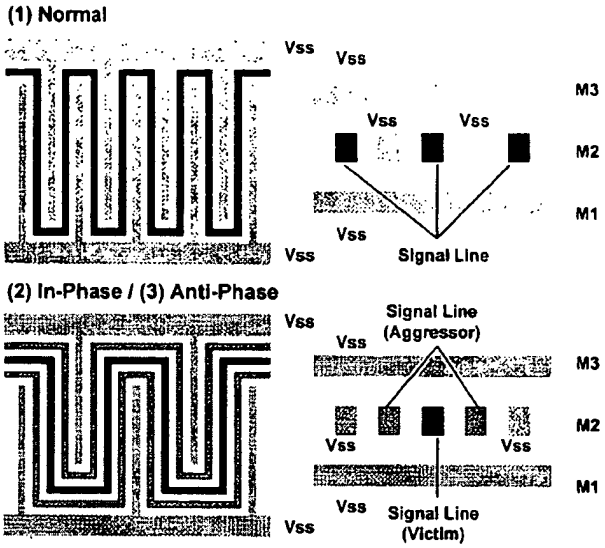


(a) Ring oscillator with wire load



(b) Schematic configurations for three signal phases (normal, in-phase and anti-phase). For in-phase, the gate is divided into fun out of 3 to drive 3 interconnects. For anti-phase, the additional inverter is required to generate the reverse signal phase on the outer lines.



(c) Schematic layout and cross section of wire load

L=S (μm)	0.25	0.50	0.75		
Lint (mm)	0.5	1.0	2.0	4.0	8.0

(d) Parameters for L=S and Lint . The variable pitches are 2 times and 3 times pitch, respectively. Interconnect length Lint is 0.5, 1, 2, 4 and 8mm to analyze the effect of the repeater.

Fig.1 Schematic of new test configurations for on-chip interconnect evaluation.

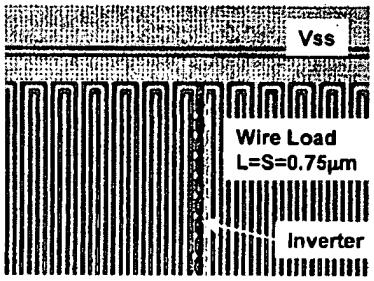


Fig.2 Test chip die photo (L=S=0.75μm wire load) . The test chip is 3.0 X 7.2 mm2 die area and it consists of 45 measurable test structures.

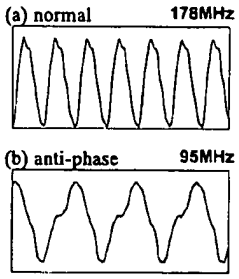


Fig.3 Measured ring oscillator waveforms for (a) normal and (b) anti-phases.

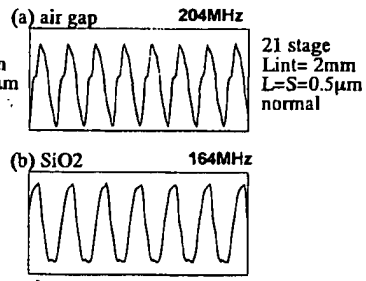


Fig.4 Measured ring oscillator waveforms for materials of (a) air gap and (b) SiO2.

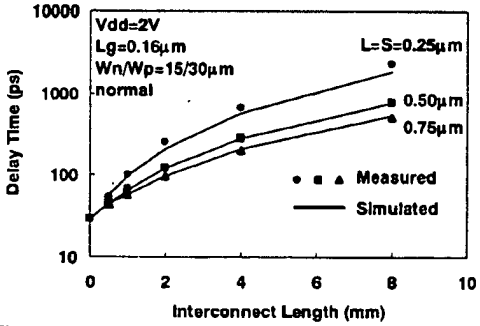


Fig.5 Measured delay time versus interconnect length at three metal pitches (L=S=0.25, 0.50 and 0.75μm).

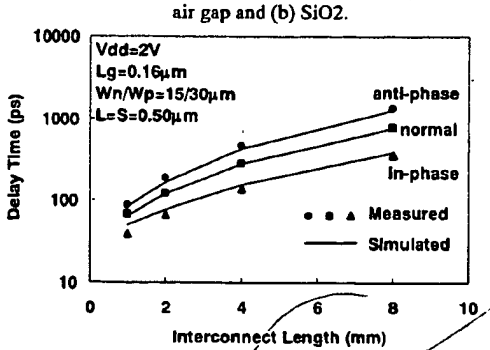


Fig.6 Measured delay time versus interconnect length for three signal phases (normal, in-phase and anti-phase).

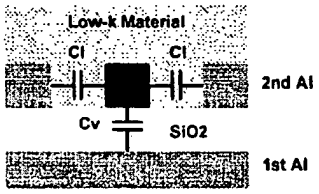


Fig.7 Schematic cross section of interconnect for evaluating the capacitance and the delay time. Cl and Cv are the lateral capacitance and the vertical capacitance, respectively. ILD processes with the materials of SiO2, organic, air-gap [5] and w. o. ILD are compared. Low-k materials are used inter line to line. Test configurations were evaluated using 2 level Al process. SiO2 is used as ILD material between 1st Al and 2nd Al.

Table.1 Interconnect Parameters used for experiments.

Dielectric constant (k)	SiO2	4.2
	organic	2.8
	air-gap	< 2.0
	without ILD	1.0
ILD thickness(1st Al and 2nd Al)		1.0 μm
Al thickness(including barrier)		0.5 μm

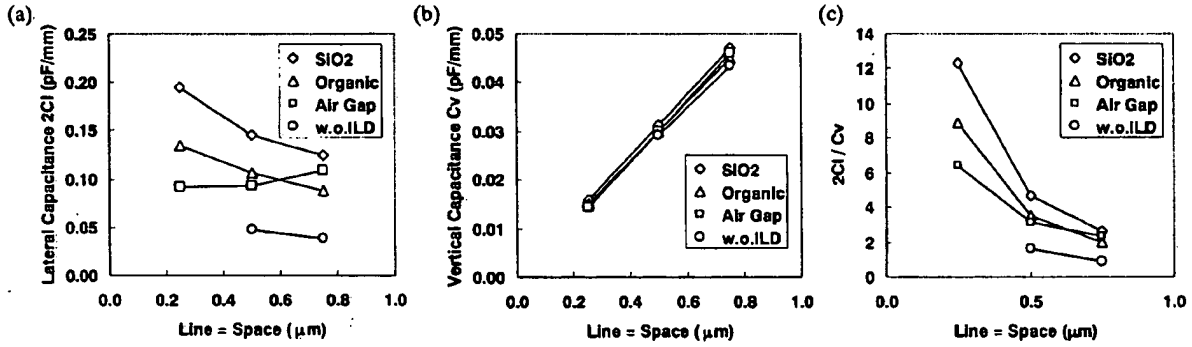


Fig. 8 Measured wiring capacitance component (a) lateral capacitance Cl, (b) vertical capacitance Cv, and (c) 2Cl/Cv for various ILD materials. Cv is almost identical for various ILD processes due to the same ILD material between 1st Al and 2nd Al. The ratio between Cl and Cv is decreased using low-k material as shown in Fig.8 (c).

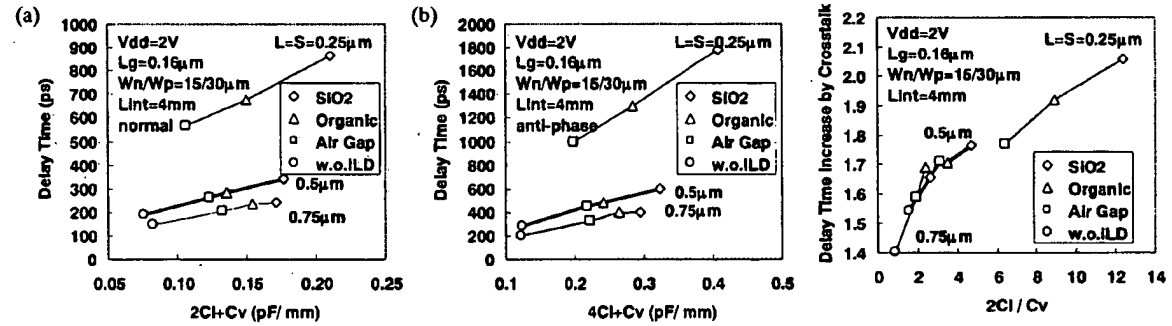


Fig.9 Measured delay time at different ILD for (a) normal case as a function of 2Cl + Cv for (b) anti-phase case as a function of 4Cl + Cv.

Fig.10 Measured delay time increase versus 2Cl/Cv for various ILD. The delay time increase is defined as normalizing of the worst case delay time (anti-phase) by the normal delay time.

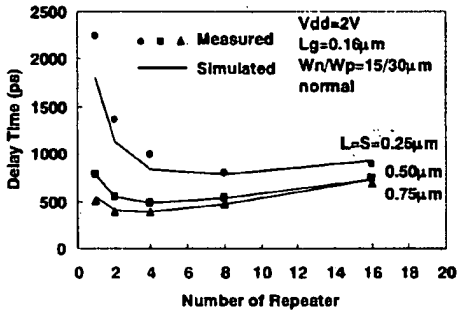


Fig.11 Delay time improvement by improved circuit design techniques (repeater and variable pitch router).

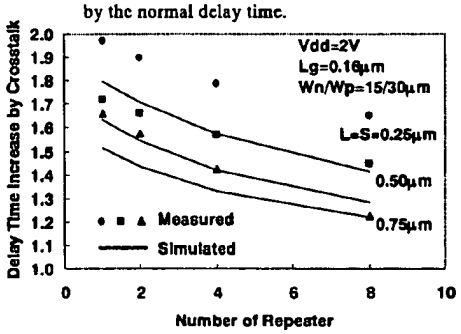


Fig.12 The reduction of delay time increase by improved circuit design techniques (repeater and variable pitch router).